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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,698	07/24/2003	Hideki Agari	R2180.0163/P163	9943

24998 7590 07/06/2005

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EXAMINER	
STERRETT, JEFFREY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,698	AGARI ET AL.	
	Examiner	Art Unit	
	Jeffrey L. Sterrett	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 2, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Geyer et al (US 6,249,110).

Geyer et al discloses a power supply apparatus comprising a first power supply circuit (LR) providing a first output voltage (5 volt) to an output terminal (A2) from an input voltage (UB) on an input terminal (A1) and a second power supply circuit (SR) providing a second output voltage (5.3 volt) to the output terminal from the input voltage on the input terminal wherein the first output voltage is smaller than the second output voltage (i.e. the first and second output voltages are unequal) and the first power supply circuit detects the output voltage in order to provide the first output voltage when the second power supply circuit is inactive (see lines 12- 23 of column 3).

3. Claims 3, 4, and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Geyer et al.

Geyer et al discloses a power supply apparatus as explained above and as recited by claims 3, 4, and 5 except for specifying the circuitry elements that comprise the first and second power supply circuits. Official notice is taken that the specific regulator topologies set forth for the first and second power supply circuits were old and known in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the power supply apparatus of Geyer et al by utilizing specific regulator topologies old and known in the art at the time of the invention for the generic first and second power supply circuits

since Geyer et al left the selection of circuit topology of the first and second power supply circuits up to the reader of the patent (see lines 60-63 of column 2,for example).

4. Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Geyer et al as applied to claim 4 above, and further in combination with Hiraki et al (US 2002/0041178).

Geyer et al discloses a power supply apparatus as explained above and as recited by claims 6 and 7 except for specifying that certain circuit elements are integrated together on a single IC. Hiraki et al discloses that integrating a select group of circuit elements of a power supply apparatus on a single IC was an old and known expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the power supply apparatus of Geyer et al by integrating a select group of the circuit elements on a single IC as disclosed by Hiraki et al in order to minimize the size of the power supply apparatus.

5. Claims 8 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Geyer et al as applied to claim 4 above, and further in combination with Hiraki et al.

Geyer et al discloses a power supply apparatus as explained above and as recited by claims 8 and 9 except for utilizing a transistor operating as a flywheel diode in the smoothing circuit. Hiraki et al discloses as an old and known in the art at the time of the invention a smoothing circuit including a flywheel diode (D1) and additionally official notice is taken that operating a transistor as a diode was an old and know expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in

the art at the time of the invention to have modified the power supply apparatus of Geyer et al by including a flywheel diode in the smoothing circuit in order to derive a desired filter characteristic as disclosed by Hiraki et al and it would have been further obvious to said skilled artisan to have also utilized a transistor operating as a diode as the flywheel diode in order to provide control over the flywheel action.

6. Claims 10 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Geyer et al as applied to claim 4 above, and further in combination with Manabe et al (US 6,236,194).

Geyer et al discloses a power supply apparatus as explained above and as recited by claims 10 and 11 except for utilizing a switching element between the outputs of the first and second power supply circuits. Manabe et al discloses as old and known in the art at the time of the invention utilizing a switching element (17) between the outputs of a first (5a) and second (5b) power supply circuits and additionally official notice is taken that utilizing a forward connected diode on the output of one of the power supply circuits to prevent reverse current flow was an old and know expedient in the art at the time of the invention as such a switching device. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the power supply apparatus of Geyer et al by utilizing a switching element between the outputs of the first and second power supply circuits in order to select one of the two power supply circuit outputs as disclosed by Manabe et al and it would have been further obvious to said skilled artisan to have also utilized a diode as a simple implementation of the switching element in order to prevent reverse current flow.

7. Claims 12-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Geyer et al in view of Manabe et al as applied to claim 10 above, and further in combination with Hiraki et al.

Geyer et al and Manabe et al collectively disclose a power supply apparatus as explained above and as recited by claims 12-15 except for specifying that certain circuit elements are integrated together on a single IC. Hiraki et al discloses that integrating a select group of circuit elements of a power supply apparatus on a single IC was an old and known expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the power supply apparatus collectively disclosed by Geyer et al and Manabe et al by integrating a select group of the circuit elements on a single IC as disclosed by Hiraki et al in order to minimize the size of the power supply apparatus.

8. Applicant's arguments filed June 3, 2005 have been fully considered but they are not persuasive.

In regards to the remarks concerning the disclosure of Geyer et al, applicant is mistaken that power supply circuits LR and SR produce the same output voltage since figure 1 clearly shows that power supply circuit LR outputs 5 volts and power supply circuit SR outputs 5.3 volts and lines 12- 23 of column 3 clearly state that a potential difference must be established between the outputs of power supply circuit LR and power supply circuit SR by utilizing outputs of 5v and 5.3v, respectively.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey L. Sterrett whose telephone number is (571) 272-2085. The examiner can normally be reached on Monday-Thursday & 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey L. Sterrett
Primary Examiner
Art Unit 2838